REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

1. Amendments to Claims

Claims 1 and 4 have been amended to recite that the deep trench communications with "only" two different active areas, as is clearly shown in Figs. 1 and 2. In addition, a typographic error in claim 4 has been corrected.

2. Rejection of Claims 1, 2, 4, and 5 Under 35 USC §102(b) in view of U.S. Patent No. 6,528,837 (Forbes)

This rejection is respectfully traversed on the grounds that the Forbes patent fails to disclose a deep trench structure that communicates with only two different active areas, which are respectively connected with two adjacent bit lines, as is now recited in claim 1. Such trench structure can facilitate measuring GIDL current and junction leakage current.

During a telephone conversation on October 12, 2005, it was determined that the Examiner considers column isolation trenches 316 shown in Fig. 5B of the Forbes patent to be the "deep trench" corresponding to the claimed "deep trench." It is respectfully submitted that this interpretation of trenches 316 of Forbes is incorrect.

As shown in Fig. 5G and described in column 8, lines 51-52 of the 837, column isolation trenches 316 are orthogonal to row isolation trenches 332. And, as shown in its Fig. 5H and described in its column 9, lines 3-8, a common plate formed by conductor mesh or grid 340 for all of the memory cells of array 299 is formed in column isolation trenches 316 and row isolation trenches 332. In other words, column isolation trenches 316 and row isolation trenches 332 communicate with each other, and therefore do not correspond to the claimed deep trench, which communicates with **only two** different active areas respectively connected with two adjacent bit lines.

Further, as shown in its Fig. 5J and described in its column 9, lines 40-44, array 299 includes memory cells 350A through 350D surrounding mesh 340. Each memory cell of memory cells 350A through 350D has an active area including layers 302, 304, and 306. Since mesh 340 is contained in column isolation trenches 316 and row isolation trenches 332, column isolation trenches 316 and row isolation trenches 332 **communicate with all of the active areas** of memory cells 350A through 350D.

Similarly, in its Fig. 3, the deep trenches containing second plate 220 (which is common to all of the capacitors of array 200) communicate with all of the active areas, including layers 206, 208, and 210, of memory cells 202A through 202D of array 200 (please refer to its column 6, line 66 through column 7, line 2). In fact, either trenches 316 and 332 containing a common plate formed by conductor mesh or grid 340 or the deep trenches containing second plate 220 communicate with all of the active areas of the memory array. As a result, the considered trenches 316 communicate with **all of the active areas, and not *only two* active areas connected with adjacent bit lines, as claimed**.

Trenches 316 described in the Forbes patent therefore have a structure substantially different from the claimed deep trench structure of the present application. Forbes clearly does not recognize the advantages of the present invention since nowhere in its specification does the Forbes patent even remotely refer to the purpose of the present application, which is to facilitate measuring GIDL current and junction leakage current.

Because the Forbes patent does not disclose all elements recited in amended claims 1, 2, 4, and 5, withdrawal of the rejection under 35 USC §102(b) is respectfully requested.

Having thus overcome each of the rejections made in the Official Action, expedited passage of the application to issue is requested.

Respectfully submitted,

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